

REMARKS

Claims 7 and 8 have been cancelled. Claims 1, 5, 9, 14, and 15 have been amended to clarify the subject matter regarded as the invention. Claims 1-6 and 9-20 are pending.

The Examiner has rejected claims 1-6 and 9-20 under 35 USC 103 as being unpatentable over Shanklin in view of Salapura and Blair.

The rejection is respectfully traversed. With respect to claims 1, 14, and 15, each has been amended to recite:

wherein the data packet is assigned to said one of said plurality of processors by storing in a work queue associated with said one of said plurality of processors a pointer to a storage location in which data comprising the data packet is stored; and the processor is configured to read the pointer, use the pointer to read the data comprising the data packet directly from the storage location in which said data comprising the data packet is stored, use the data comprising the data packet to perform a network flow analysis with respect to a network flow with which the data packet is associated, and store in a return queue associated with the processor a data indicating that the processor is finished processing the data comprising the data packet; and wherein the data indicating that the processor is finished processing the data comprising the data packet is used to determine that the storage location is available to be used to store a subsequently received data comprising a subsequently received data packet.

Support for the above amendment to claims 1, 14, and 15 is found, without limitation, in the present application at page 17, lines 3-12; page 17, line 18 – page 18, line 11; page 18, line 19 – page 19, line 1; and page 21, lines 5-14.

Of Shanklin, Salapura, and Blair only Salapura describes direct memory access by multiple processors of a shared host memory. However, none of the references describes a multiple processor system in which each processor is configured to “perform network flow analysis with respect to a network flow” with which a packet read directly from shared host memory is associated, as recited in claims 1, 14, and 15. In addition, none teaches a processor configured to “store in a return queue associated with the processor a data indicating that the processor is finished processing the data comprising the data packet” which data is then “used to determine that the storage location is available to be used to store a subsequently received data comprising a subsequently received data packet,” as recited in claims 1, 14, and 15. The return

queue approach described in the present application and recited in claims 1, 14, and 15 enables memory to be freed quickly for reuse and avoids having any component wait for any other because each processor stores pointer information in its own return queue independently of the others and the information is read from the respective work queues asynchronously. See, e.g., Application at page 17, lines 3-9 and page 18, line 19 – page 19, line 14. As such, claims 1, 14, and 15 are believed to be allowable.

Claims 2-6 and 9-13 depend from claim 1 and are believed to be allowable for the same reasons described above. Likewise, claims 16-20 depend from claim 15 and are believed to be allowable for the same reasons described above.

The foregoing amendments are not to be taken as an admission of unpatentability of any of the claims prior to the amendments.

Reconsideration of the application and allowance of all claims are respectfully requested based on the preceding remarks. If at any time the Examiner believes that an interview would be helpful, please contact the undersigned.

Respectfully submitted,

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